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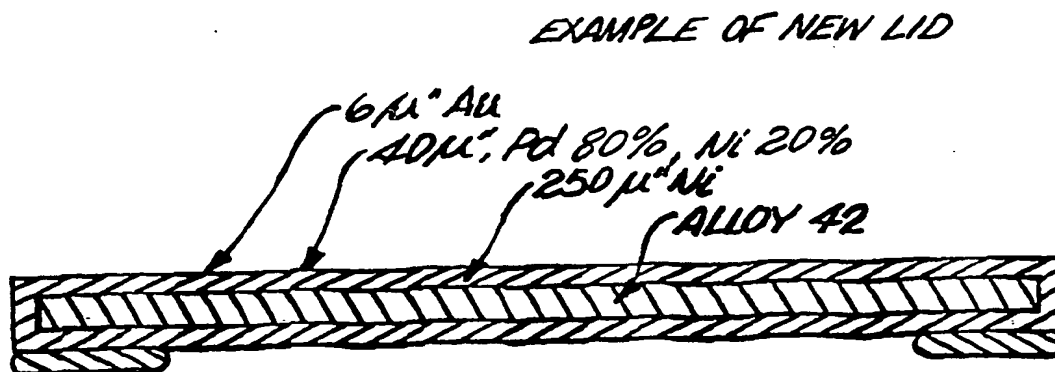
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(54) Title: METAL COVER FOR CERAMIC PACKAGE AND METHOD OF MAKING SAME



(57) Abstract

A solderable metallic cover for hermetically sealing a ceramic package that includes an iron or iron-alloy core and layers of nickel or nickel alloy on the core and palladium or palladium alloy on the nickel layer.

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METAL COVER FOR CERAMIC PACKAGE  
AND METHOD OF MAKING SAME

Background of the Invention

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1. Field of the Invention

This invention relates to a sealing cover which is particularly suitable for sealing ceramic packages for semiconductor devices, and to a method of producing the same.

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2. Description of the Prior Art

The use of ceramic packages for semiconductor devices is well-known. Typically, such a package includes a ceramic container to which the cover must be sealed. Sealing covers, also known as "lids," of the type used in connection with containers for semiconductor devices are well known and typically include one or more layers of gold, often of substantial thickness, to aid in corrosion resistance as well as to provide for electrical connection of leads. Such covers are not only expensive but also introduce a possible health hazard, since cyanide solutions are often used in gold plating.

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The present invention is directed to a novel sealing cover, and to a method of making same, which avoids or at least substantially reduces the use of gold, thus lowering cost and reducing potential health hazards by eliminating or greatly minimizing gold plating. By eliminating or

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1 minimizing use of gold, material and manufacturing costs  
related to the production of lids for semiconductor  
packages can be significantly lowered. In accordance with  
the present invention, a sealing cover is provided which  
5 is not only economical because it replaces gold with  
palladium, but is also of sufficiently high quality to  
pass standard tests for temperature cycling and thermal  
shock as well as resistance to corrosion in a salt  
atmosphere.

10 Although use of palladium in the manufacture of  
sealing covers is known, such use has been primarily  
limited to palladium in the form of palladium-silver paste  
applied to ceramic lids. This use merely takes advantage  
of the ability of palladium to fuse to ceramic in paste  
15 form. However, even in such uses only small quantities of  
palladium paste are employed, generally around the  
perimeter of the cover, and the use of palladium in this  
manner does not materially reduce or affect the overall  
manufacturing costs.

20 Miyoshi, et al. U.S. Patent No. 4,640,436 has  
suggested the use of a coating of gold, palladium, silver  
or platinum on a solder ring to assist in diffusion  
bonding of the solder to the lid. In this case, the lid  
is plated with "a material of high solderability" such as  
25 gold. In Levine U.S. Patent Nos. 4,835,067 and 4,666,796,  
it is suggested to use palladium as a solderable coating  
on a metal lid as two distinct layers of palladium with a  
layer of a more reactive metal sandwiched between the two  
palladium layers. Patentee provides this structure to  
cancel the galvanic effect that the noble top layer would  
30 normally have on the iron-based substrate to which the  
layers are applied to avoid a possible "short circuit"  
created if the iron and gold become connected through  
pinholes in an intermediate layer.

35 The present invention differs from the prior art, and  
in particular the disclosures in the Levine patents, in  
that the present invention involves a metallic cover,

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1 preferably with an iron-alloy core, and not a ceramic  
cover. Therefore, there is no need to coat the solder  
with palladium. The new sealing cover employs separate  
distinct layers without alternating the layers according  
5 to the EMF value of the coatings and only a single  
palladium-containing layer is employed. Surprisingly, the  
relatively simple construction of the cover of the present  
invention still imparts sufficient corrosion resistance in  
salt atmospheres while retaining its solderability, but at  
10 a substantially reduced cost over the gold-containing  
sealing covers heretofore known.

#### Summary of the Invention

15 In accordance with the invention, there is provided  
a metallic cover for hermetically sealing a semiconductor  
device package by soldering, which includes a substrate  
comprising a core of iron alloy, a first layer on the core  
which comprises nickel or nickel alloy, and a second layer  
on the first layer which comprises palladium or palladium  
20 alloy. To provide a cover which resembles those currently  
used, a coating of gold may be applied as an outer layer,  
but such a layer would be significantly thinner than that  
conventionally used. However, in many applications the  
layer of gold may be eliminated altogether without  
25 adversely affecting the desirable characteristics of the  
cover. The sealing cover of the invention may be made by  
providing a core of an iron alloy, such as iron-nickel  
alloy, applying a first layer comprising a nickel or  
nickel alloy onto the core and then applying a second  
30 layer comprising palladium or palladium alloy onto the  
first layer. Optionally, a final thin coating of gold may  
be applied onto the second layer.

A semiconductor device package may be assembled using  
a cover as described by soldering it to a ceramic  
35 enclosure having a semiconductor device therein to  
hermetically seal the package, with a gold-free solder  
selected from the group consisting of solders containing

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1 at least one of lead, tin, silver, indium, bismuth,  
palladium, platinum and antimony, and which has a melting  
point in the range of from about 220°C to 300°C to avoid  
5 exposing the semiconductor device therein to elevated  
temperatures that might damage the device. The solder may  
be incorporated as a solder preform of suitable  
configuration. In this manner, a soldered hermetically  
sealed semiconductor package may be assembled using the  
sealing cover and method previously described.

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1     Brief Description of the Drawings

5             FIG. 1 is a schematic cross-sectional view of a  
sealing cover showing a metallic core over which is  
applied a nickel-containing coating and a final gold layer  
over the nickel-coated core; and

           FIG. 2 is a schematic representation of a sealing  
cover in accordance with the invention.

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1     Detailed Description of the Invention

          In the sealing cover construction described in FIG. 1, the final layer consists of a substantially thick layer of gold. If it is possible to reduce the thickness  
5     of the gold coating or eliminate it altogether, while retaining the required characteristics of corrosion-resistance, etc. a significant reduction in manufacturing costs would occur. This is accomplished by the cover described in FIG. 2, which is an example of the invention  
10     wherein a metallic core is coated with a nickel-containing material, but a palladium-containing layer is applied onto the nickel layer. The use of palladium or a palladium alloy in this manner avoids the need for a thick outer layer of gold and, for many applications, allows the gold  
15     layer to be omitted altogether. The term "palladium alloy" as used herein refers to an alloy in which palladium is a major constituent and present in an amount of at least about 30 wt.%.

          In accordance with the presently preferred embodiment  
20     of the invention, a suitable metallic core, such as one made of iron-nickel alloy, known as "Alloy 42," "Alloy 45" or "Alloy 46" or the alloy known as "Kovar," may be provided. Alloys 42, 45 and 46 refer to compositions containing 42, 45 and 46 wt.% nickel, respectively. The  
25     particular composition of the core is not critical to the success of the cover of the invention and any iron-based alloy may be used for this purpose provided similar thermal expansion characteristics to ceramic is maintained.

30     A first layer of nickel or nickel alloy is applied to the core. The nickel-containing material may be applied as an electrolytic or "electroless" coating. Presently, an electrolytic nickel-containing coating is preferred, because it appears to provide good corrosion resistance  
35     and economical and repeatable manufacture process. In lieu of a nickel or nickel alloy, a first layer of tin, silver, cadmium, indium, lead, copper, cobalt, ruthenium,



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1        iridium, zinc, or their alloys, may be employed. However,  
it has been determined that nickel and nickel alloys are  
preferred for their combination of cost, relative ease of  
application and resistance to corrosion.

5        The thickness of the first layer is very important in  
producing a sealing cover with desirable properties. It  
has been determined that the thickness of the  
nickel/nickel-alloy layer should be in the range of 100 to  
800  $\mu$ in. Although performance characteristics equal to  
10       that obtained with present technology can be achieved with  
as little as 100  $\mu$ in, a cover with superior properties is  
not achieved until the minimum thickness of the  
nickel/nickel-alloy layer is in the range of 400 to  
600  $\mu$ in. The nominal thickness of this layer is  
15       advantageously about 500  $\mu$ in.

As a second layer, it is important to use a layer of  
palladium or palladium alloy (as defined previously), and  
in particular, a palladium-nickel alloy. The most  
preferred composition presently is an alloy of about 80%  
20       palladium and about 20% nickel; however, alloys of at  
least about 30 wt.% palladium, balance nickel, silver or  
tin, are also particularly advantageous. In lieu of  
palladium and palladium alloys as aforesaid, however, it  
may be possible to use tin, platinum, silver, cadmium,  
25       indium, cobalt, lead, rhodium, ruthenium, iridium, or  
their alloys, and alloys of palladium with the foregoing.  
The thickness of the palladium-containing layer is not as  
critical as the thickness of the first layer to achieving  
desirable properties in the sealing cover. However, it  
30       has been determined that the palladium-containing layer  
should be present in a range of from 10  $\mu$ in to 100  $\mu$ in for  
maximum performance. Although performance characteristics  
equal to covers made with present technology could be  
achieved with as little as 10  $\mu$ in, if the first layer is  
35       sufficiently thick, i.e., at least 400 to 600  $\mu$ in of  
electrolytic nickel, superior performance may be achieved  
with a palladium-containing layer in the range of 20 to

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1        60  $\mu$ in.    The improvement in performance of a cover  
employing a second layer of palladium-containing alloy is  
believed to be related to the statistical probability that  
each successive layer of plating will cover over porosity  
5       defects in the lower layer.    Even though each such  
successive layer may have its own channel sites, the  
probability that defect sites will coincide with defects  
in other layers is very small.    Palladium and palladium-  
containing alloys are preferred because of their excellent  
10       solderability characteristics and the ability of such  
materials to supplement the ability of the first layer to  
minimize pinhole pores which create paths between the  
iron-containing core and the surrounding, possibly  
corrosive, atmosphere.

15       Optionally, a coating of gold may be applied to the  
palladium-containing layer to provide an outer-surface  
appearance resembling sealing covers currently in use,  
which would improve the acceptability of the sealing cover  
in the marketplace.    Some additional advantage may result  
20       from the application of the thin layer of gold by  
assisting tack welding of a preform to the lid.  
Substitutes for gold in this application may include tin,  
palladium, platinum, silver, cadmium, indium, cobalt,  
lead, rhodium, ruthenium, indium, and their alloys.

25       Desirably, the gold layer is present in the range of  
from 0 to less than 50  $\mu$ in.    Performance characteristics  
equal to covers made with present technology can be  
achieved without the gold layer if the second layer is a  
palladium-containing material of sufficient thickness,  
30       e.g., at least 50  $\mu$ in, and the first layer is a nickel-  
containing layer also of sufficient thickness, e.g., at  
least 500  $\mu$ in.    As an example, superior performance may be  
achieved with a nominal gold thickness of 10  $\mu$ in, which is  
believed sufficient to enhance solderability and cover  
35       pinhole pores which may be present in the first and/or  
second layers.

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1 In order to determine the optimum combinations of  
 materials to function as the layers in the above-described  
 sealing cover, the following combinations of plating  
 solutions and coatings were investigated as potential  
 5 replacements for the standard nickel-and-gold-plated lid  
 to determine if they may be used to produce a sealing  
 cover that exhibits the same functional characteristics  
 but at reduced cost. Obviously, the combinations  
 including gold are more expensive than the gold-free  
 10 combinations. The materials investigated appear in  
 Table 1.

TABLE I

	<u>Sample I.D.</u>	<u>Metallization</u>	<u>Thickness</u>
15	A1	Matte Sulfamate Nickel	(250 $\mu$ in)
		Pure Gold	( 50 $\mu$ in)
	A2	Matte Sulfamate Nickel	(250 $\mu$ in)
		Palladium/Nickel	( 50 $\mu$ in)
	A3	Matte Sulfamate Nickel	(250 $\mu$ in)
		Palladium/Nickel	( 50 $\mu$ in)
		Pure Gold	( 7 $\mu$ in)
20	A4	Matte Sulfamate Nickel	(250 $\mu$ in)
		Tin/Zinc	(100 $\mu$ in)
	B1	Electroless Nickel	(250 $\mu$ in)
		Pure Gold	( 50 $\mu$ in)
	B2	Electroless Nickel	(250 $\mu$ in)
		Palladium/Nickel	( 50 $\mu$ in)
	B3	Electroless Nickel	(250 $\mu$ in)
		Palladium/Nickel	( 50 $\mu$ in)
25		Pure Gold	( 7 $\mu$ in)
	B4	Electroless Nickel	(250 $\mu$ in)
		Tin/Zinc	(100 $\mu$ in)
	C1	Electroless Nickel	(150 $\mu$ in)
		Matte Sulfamate Nickel	(100 $\mu$ in)
		Pure Gold	( 50 $\mu$ in)
	C2	Electroless Nickel	(150 $\mu$ in)
30		Matte Sulfamate Nickel	(100 $\mu$ in)
		Palladium/Nickel	( 50 $\mu$ in)
	C3	Electroless Nickel	(150 $\mu$ in)
		Matte Sulfamate Nickel	(100 $\mu$ in)
		Palladium/Nickel	( 50 $\mu$ in)
		Pure Gold	( 7 $\mu$ in)
	C4	Electroless Nickel	(150 $\mu$ in)
35		Matte Sulfamate Nickel	(100 $\mu$ in)
		Tin/Zinc	(100 $\mu$ in)
	D1	Semi-bright Sulfamate Ni	(125 $\mu$ in)
		Matte Sulfamate Nickel	(125 $\mu$ in)
		Pure Gold	( 50 $\mu$ in)

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1	D2	Semi-bright Sulfamate Ni	(125 $\mu$ in)
		Matte Sulfamate Nickel	(125 $\mu$ in)
		Palladium/Nickel	( 50 $\mu$ in)
	D3	Semi-bright Sulfamate Ni	(125 $\mu$ in)
		Matte Sulfamate Nickel	(125 $\mu$ in)
		Palladium/Nickel	( 50 $\mu$ in)
5	D4	Pure Gold	( 7 $\mu$ in)
		Semi-bright Sulfamate Ni	(125 $\mu$ in)
		Matte Sulfamate Nickel	(125 $\mu$ in)
	E1	Tin/Zn	(100 $\mu$ in)
		Palladium/Nickel	( 10 $\mu$ in)
		Matte Sulfamate Nickel	(240 $\mu$ in)
10	E2	Pure Gold	( 50 $\mu$ in)
		Palladium/Nickel	( 10 $\mu$ in)
		Matte Sulfamate Nickel	(140 $\mu$ in)
	E3	Palladium Nickel 80/20	( 30 $\mu$ in)
		Palladium/Nickel	( 10 $\mu$ in)
		Matte Sulfamate Nickel	(140 $\mu$ in)
15	E4	Palladium Nickel 80/20	( 30 $\mu$ in)
		Pure Gold	( 7 $\mu$ in)
		Palladium/Nickel	( 10 $\mu$ in)
	F1	Matte Sulfamate Nickel	( 10 $\mu$ in)
		Tin/Zinc	(100 $\mu$ in)
		Electroless Nickel	(500 $\mu$ in)
20	F2	Pure Gold	( 50 $\mu$ in)
		Electroless Nickel	(500 $\mu$ in)
		Palladium/Nickel	( 50 $\mu$ in)
	F3	Electroless Nickel	(500 $\mu$ in)
		Palladium/Nickel	( 50 $\mu$ in)
		Pure Gold	( 7 $\mu$ in)
25	F4	Electroless Nickel	(500 $\mu$ in)
		Tin/Zinc	(100 $\mu$ in)
		Matte Sulfamate Nickel	(500 $\mu$ in)
	G3	Palladium/Nickel	( 50 $\mu$ in)
		Pure Gold	( 7 $\mu$ in)
		Electroless Nickel	(500 $\mu$ in)
25	H3	Palladium/Nickel	( 50 $\mu$ in)
		Pure Palladium	( 10 $\mu$ in)
		Electroless Nickel	(500 $\mu$ in)
	H4	Pure Palladium	( 50 $\mu$ in)
		Electroless Nickel	(500 $\mu$ in)
		Pure Palladium	( 50 $\mu$ in)

Of the foregoing, the samples which outperformed covers made by present technologies with respect to salt atmosphere corrosion resistance were:

35	F2	Electroless Nickel	(500 $\mu$ in)
		Palladium/Nickel	( 50 $\mu$ in)
		Electroless Nickel	(500 $\mu$ in)
	F3	Palladium/Nickel	( 50 $\mu$ in)
		Pure Gold	( 7 $\mu$ in)
		Electroless Nickel	(500 $\mu$ in)

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1	G3	Matte Sulfamate Nickel	(500 $\mu$ in)
		Palladium/Nickel	( 50 $\mu$ in)
		Pure Gold	( 7 $\mu$ in)
	H3	Matte Sulfamate Nickel	(500 $\mu$ in)
		Palladium/Nickel	( 40 $\mu$ in)
		Pure Palladium	( 10 $\mu$ in)
5	H4	Matte Sulfamate Nickel	(500 $\mu$ in)
		Pure Palladium	( 50 $\mu$ in)

From investigation of the above combinations, it was determined that the materials of samples G3 and A3 produced the most satisfactory results. Therefore, these samples were scaled up to normal production-size baths of 25 gallons and production runs were conducted to confirm the improvements obtained. The following example describes a typical plating sequence and the plating parameters of each step of the preferred process. The load size in each case was 300g of 0.605 x 0.605 lids, using a standard barrel, Sterling Model 46.

Step 1 ALKALINE ELECTRO-CLEANER

20	Product	Alkaline soap cleaner, e.g., Micel's X-Cel-133
	Concentration	0.5 lbs/gal
	Solution temperature	150°F
	Current	Cathodic at 4 volts
	Exposure time	10 minutes

25 Step 2 D.I. WATER RINSE

Exposure time	10 minutes
---------------	------------

Step 3 ACID ACTIVATOR

30	Hydrochloric acid	30% by volume
	Solution temperature	Ambient
	Exposure time	10 minutes

Step 4 D.I. WATER RINSE

Exposure time	2 minutes
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- 1        Step 5    Alternate A  
                 ELECTROLYTIC NICKEL
- |   |                      |                        |
|---|----------------------|------------------------|
|   | Product              | Matte sulfamate nickel |
|   | Nickel concentration | 0.5 lbs/gal            |
|   | Nickel bromide       | 2.0 oz/gal             |
| 5 | Boric acid           | 4.0 oz/gal             |
|   | pH                   | 4.3                    |
|   | Solution temperature | 130°F                  |
|   | Current              | 12 amperes             |
|   | Deposition Rate      | 90 $\mu$ in/hour       |
- 10       Step 5    Alternate B  
                 MID-PHOS ELECTROLESS NICKEL
- |    |                      |                             |
|----|----------------------|-----------------------------|
|    | Product              | Mid-Phos electroless nickel |
|    | Nickel concentration | 0.5 lbs/gal                 |
|    | pH                   | 5.0                         |
|    | Solution temperature | 150°F                       |
| 15 | Deposition Rate      | 350 $\mu$ in/hour           |
- 15       Step 6    D.I. WATER RINSE
- |  |               |           |
|--|---------------|-----------|
|  | Exposure time | 2 minutes |
|--|---------------|-----------|
- 20       Step 7    ACID ACTIVATOR
- |  |                      |               |
|--|----------------------|---------------|
|  | Hydrochloric acid    | 30% by volume |
|  | Solution temperature | Ambient       |
|  | Exposure time        | 10 minutes    |
- 25       Step 8    D.I. WATER RINSE
- |  |               |          |
|--|---------------|----------|
|  | Exposure time | 1 minute |
|--|---------------|----------|
- 25       Step 9    PALLADIUM/NICKEL ALLOY
- |    |                         |                  |
|----|-------------------------|------------------|
|    | Product                 | 80% Pd - 20% Ni  |
|    | Palladium concentration | 0.5 lbs/gal      |
|    | Nickel concentration    | 2.0 oz/gal       |
|    | Deposit modifier        | 1.0% by vol      |
|    | Stress reducer          | 1.0% by vol      |
| 30 | pH                      | 8.5              |
|    | Solution temperature    | 90°F             |
|    | Current                 | 6.1 amperes      |
|    | Deposition Rate         | 30 $\mu$ in/hour |
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1      Step 10 Alternate A  
          PURE GOLD

	Product	Mil. Spec. G-45204, Type 3, Grade A. pure gold
5	Gold concentration	0.75 oz/gal
	Additive T concentration	1.0% by vol
	Stabilizer	12% by vol
	Baume	16°
	pH	6.8
	Solution temperature	110°F
	Current	1 amperes
10	Deposition Rate	30 $\mu$ in/hour

         Step 10 Alternate B  
          PURE PALLADIUM

	Product	100% Pd.
	Palladium concentration	10 g/l
	Additive concentration	50 g/l
15	Brightener	0.5% by volume
	Baume	16°
	pH	9.5
	Solution temperature	120°F
	Current	1 amperes
	Deposition Rate	30 $\mu$ in/hour

20                    Evaluation of sealing covers produced in accordance  
 with the invention has indicated that the preferred  
 material for the core of the cover is an iron-nickel  
 alloy, such as Alloy 42, Alloy 45, Alloy 46 or Kovar. The  
 preferred composition of the first layer is electrolytic  
 25    or electroless nickel and/or nickel alloy, with  
 electrolytic nickel and/or nickel alloy considered most  
 advantageous. Preferably, the palladium-containing layer  
 is formed of a palladium-nickel alloy, optimally 80%  
 palladium and 20% nickel, or 30 to 100% palladium with  
 30    silver or tin.

                  The sealing cover is hermetically sealed to the  
 ceramic package by soldering. Advantageously, to reduce  
 costs, it is desirable to employ a gold-free or  
 substantially gold-free solder for this purpose. It has  
 35    been determined that the gold-free solder should be one  
 selected from the group consisting of solders containing

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1 at least one of lead, tin, silver, palladium platinum,  
indium, bismuth and antimony, but which have a melting  
point in the range of about 220°C to 300°C. These  
relatively low melting-point solders are additionally  
5 preferred so as to avoid the necessity of exposing the  
semiconductor device within the package to elevated  
temperatures, such as might possibly injure the  
semiconductor. More advantageously, preferred  
compositions include solders containing in wt.% about 75%  
10 tin, about 20% silver and about 5% antimony; solders  
containing about 84.5% lead, 5.5% indium, 5% tin, 3%  
antimony and 2% silver; and solders containing up to about  
95% lead, preferably not less than 90% lead, up to about  
5% palladium and which may additionally include up to  
15 about 5% silver, up to about 5% bismuth, up to about 5%  
antimony, and up to about 5% gold or a mixture of gold and  
tin having up to about 5% gold and up to about 2% tin.  
Other useful solders include 95% Pb-5% Pt.

To further illustrate solders useful in accordance  
20 with the present invention, 12 solder compositions shown  
in the following table have been prepared:

25

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	solder comp'n	Pb	Sn	Ag	In	Bi	Sb	Pt	Pd	Au
1	1		75.0	20.0			5.0			
5	2		80.0	10.0			10.0			
	3	84.5	5.0	2.0	5.5		3.0			
	4	88.0	4.5	2.5	5.0					
10	5	95.0						5.0		
	6	95.0							5.0	
	7	90.0	1.0						5.0	4.0
	8	93.0	0.5						5.0	1.5
15	9	90.0		5.0					5.0	
	10	90.0				5.0			5.0	
	11	90.0			5.0				5.0	
20	12	93.0					2.0		5.0	

Ceramic packages with sealing covers as described herein have been found to be capable of passing Mil. Std. 883C, Method 1010 for Test Condition C, 1,000 x temperature cycles and thermal shock testing. In addition, the essentially three-layer cover described herein is also able to pass salt-atmosphere testing, is very solderable and cosmetically identical to the lid described in Mil-M-38510G (50 to 350  $\mu$ in nickel under 50 to 225  $\mu$ in gold), with all the same physical properties, but at a much reduced cost.

Resistance to corrosion in a salt atmosphere is generally measured as a percentage of surface area which is corroded. Sealing covers of the present invention have less than 1% corrosion and preferably, less than 1/2%

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1 corrosion, in terms of surface area, as determined according to Mil-Std-883, Method 1009.9, Condition A.

5 In the conventional lid combining a first nickel layer on an iron-nickel core and an outer gold layer, the first layer is nominally 250  $\mu$ in and the gold layer is 50  $\mu$ in. The usual test to measure salt atmosphere corrosion resistance involves exposing 25 test pieces at a time. Corrosion resistance of convention covers exhibit test results showing < 1% surface area corrosion, with an average of about 0.25% surface area corrosion. In contrast, comparable tests of 25 pieces of 500  $\mu$ in Ni on an iron-nickel alloy core with 40  $\mu$ in Pd-Ni alloy and 5  $\mu$ in Au results in < 0.5% surface area corrosion and an average of about 0.1%.

15 The following is an example of one preferred embodiment. A core of "Alloy 42" is spot welded to a solder ring. Three steps are used to fabricate a complete lid.

- 20 A. Plated lid production.
  - B. Solder ring production and punching.
  - C. Attachment of the solder ring to the plated lid.
- Each process is described in detail below.

**A. Plated Lid Production**

25 Alloy 42 (Fe 58%, Ni 42%) is rolled into sheets 0.010" to 0.015" thick, and annealed into a state making it suitable for punching (typically 95,000 psi tensile strength). The sheet is slit into coils wide enough to make them easily punched through a progressive die set.

30 Using standard technology this material is then punched into sizes suitable for sealing onto ceramic packages. Typical sizes include:

.250"	x	.375"	x	0.010"
.505"	x	.505"	x	0.010"
.860"	x	.860"	x	0.015"

35 The punched squares may then be deburred chemically or mechanically to clean up any rough edges that may result from metal shearing.

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1           The cleaned and deburred lids may then be loaded into  
a plating barrel for degreasing, oxide removal, and  
electroplating of all desired layers. One barrel of low  
cost lids were plated using the following sequence:

5           1. A Sterling System 6" x 12" plating barrel was  
loaded about 30% full with .605" x .605" x 0.010" alloy 42  
squares which had been previously punched and deburred in  
the manner described above.

10          2. This barrel was plated with nickel, palladium-  
nickel and gold using the following sequence:

- a. Electroclean at 5 volts anodic for 5 minutes;
- b. Rinse for at least 5 minutes;
- c. Descale in acid blend for 5 minutes;
- 15       d. Rinse for 2 minutes;
- e. Plate in Sulfamate Nickel for ample time to deposit 500  $\mu$ in;
- f. Rinse for 5 minutes;
- g. Acid activate in 5% HCl (optional);
- 20       h. Plate in Pd-Ni for ample time to deposit 40  $\mu$ in;
- i. Rinse for 5 minutes;
- j. Plate in a high adhesion pure gold bath for ample time to deposit 5  $\mu$ in 99.9% pure gold;
- 25       k. Rinse for 10 minutes in warm cascading deionized water; and
- l. Dry in TDFC Freon dryer or suitable substitute.

30          3. Lids electroplated in the manner described will  
routinely pass the following tests:

- a. A 450°C five-minute bake in air;
- b. A corrosion test permit std 883c., method 1009 condition A; and
- 35       c. A visual test for stains, blisters, or poor adhesion.

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1     **B. Solder Ring Production and Punching**

      A predetermined quantity 99.99% pure lead is brought  
to its melting point in a bottom draw continuous caster.  
To the molten lead is added 5.0 wt.% 99.99% pure palladium  
5     in powder form. After allowing ample time for the mixture  
to alloy, the metal is cast continuous style through a  
0.200" x 2.000" die. (Other size die are also suitable.)

      The resulting 0.200" x 2.000" piece is rolled down to  
a thickness of 0.0021" +/- 0.003" over 12 passes at room  
10    temperature. A petroleum based oil is used as a  
lubricant.

      After removal of the rolling oil with naphtha and  
methylene chloride, the clean strip is punched into  
"window frame" shapes 0.0021" thick x 0.605" OD x 0.505"  
15    ID. A compound punching die set is used, and although the  
material deforms easily, several thousand pieces are made  
in this manner.

      A final wash in Freon or another suitable solvent is  
optional at this stage, although it has been found not to  
20    be necessary.

**C. Attachment of the Solder Ring to the Plated Lid**

      Appropriate tooling for fastening the solder window  
frames of step B to the plated alloy 42 lids of step A is  
performed by methods known to the trade and typically  
25    produced by specialty manufacturers, usually by resistance  
welding.

      The tooling used for this work is generally  
insulating platform with 8 pins arranged to hold the lid  
and solder ring in alignment. Arranged 0.025" in from  
30    each corner in the block is an electrode extending 0.005"  
out of the block.

      By clamping the assembly in place from above, it is  
possible to spot weld the lid to the solder by passing a  
high current through the electrodes.

35    This lid-solder combination is the finished product  
which may be used to hermetically seal a silicon die into  
a ceramic package.

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1           In view of the foregoing description, it is  
apparent that various changes and modifications may be  
made without departing from the invention. Accordingly,  
the scope of the invention should be limited only by the  
5           appended claims.

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## 1      WHAT IS CLAIMED IS:

1.      A solderable metallic cover for hermetically  
sealing a package containing a semiconductor device  
5      comprising a core of iron or iron-nickel alloy, a first  
layer on said core comprising nickel, tin, silver,  
cadmium, indium, lead, copper, cobalt, ruthenium, iridium,  
zinc, and alloys thereof, and a second layer on said first  
layer comprising palladium, tin, platinum, silver,  
10      cadmium, indium, cobalt, lead, rhodium, ruthenium,  
iridium, and alloys thereof, and a layer of gold on said  
second layer of a thickness of 0 to 50  $\mu$ in.

2.      A solderable metallic cover for hermetically  
15      sealing a package containing a semiconductor device  
comprising a core of iron or iron-nickel alloy, a first  
layer on said core comprising nickel or nickel alloy, and  
a second layer on said first layer comprising palladium or  
palladium alloy and a layer of gold on said second layer  
20      of a thickness of 0 to 50  $\mu$ in.

3.      A cover according to claim 2 wherein said  
substrate comprises one of Alloy 42, Alloy 45, Alloy 46 or  
Kovar.

25

4.      A cover according to claim 2 wherein said first  
layer comprises one from the group consisting of  
electrolytic and electroless nickel and alloys of nickel  
of a thickness of 100 to 800  $\mu$ in.

30

5.      A cover according to claim 4 wherein said first  
layer is 400 to 600  $\mu$ in.

6.      A cover according to claim 2 wherein said second  
35      layer comprises at least about 30 wt.% palladium, the  
balance nickel, silver or tin.

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1           7. A cover according to claim 2 wherein said second layer comprises an alloy of palladium and nickel.

5           8. A cover according to claim 6 wherein said second layer comprises 10 to 100  $\mu$ in of one from the group consisting of palladium and alloys of palladium.

10           9. A cover according to claim 8 wherein said second layer comprises 20 to 60  $\mu$ in.

15           10. A cover according to claim 6 wherein said second layer comprises an alloy of about 80% palladium and about 20% nickel, by weight.

20           11. A method of assembling a semiconductor device package comprising soldering a cover according to claim 1 to a ceramic enclosure having a semiconductor device therein to hermetically seal said package with a gold-free solder selected from the group consisting of solders containing at least one of Pb, Sn, Ag, In, Bi, Pd, Pt and Sb, and which has a melting point in the range of from about 220°C to 300°C.

25           12. A method according to claim 11 wherein said solder comprises in wt.% about 75% Sn, about 20% Ag and about 5% Sb.

30           13. A method according to claim 11 wherein said solder comprises in wt.% about 84.5% Pb, about 5.5% In, about 5% Sn, about 3% Sb and about 2% Ag.

14. A method according to claim 11 wherein said solder comprises about 95% Pb and about 5% Pd.

35           15. A method according to claim 11 wherein said solder comprises up to about 95% Pb, up to about 5% Pd, up to about 5% Ag, up to about 5% Bi, up to about 5% Sb, up

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1 to 5% Au, and up to about 7% of a mixture of Au and Sn  
having up to about 5% Au and up to 2% Sn.

5 16. A method of assembling a semiconductor device  
package comprising soldering a cover according to claim 2  
to a ceramic enclosure having a semiconductor device  
therein to hermetically seal said package with a gold-free  
solder selected from the group consisting of solders  
10 containing at least one of Pb, Sn, Ag, In, Bi, Pd, Pt and  
Sb, and which has a melting point in the range of from  
about 220°C to 300°C.

15 17. A method according to claim 16 wherein said  
solder comprises in wt.% about 75% Sn, about 20% Ag and  
about 5% Sb.

20 18. A method according to claim 16 wherein said  
solder comprises in wt.% about 84.5% Pb, about 5.5% In,  
about 5% Sn, about 3% Sb and about 2% Ag.

19. A method according to claim 16 wherein said  
solder comprises about 95% Pb and about 5% Pd.

25 20. A method according to claim 16 wherein said  
solder comprises up to about 95% Pb, up to about 5% Pd, up  
to about 5% Ag, up to about 5% Bi, up to about 5% Sb, up  
to 5% Au, and up to about 7% of a mixture of Au and Sn  
having up to about 5% Au and up to 2% Sn.

30 21. A method of making a cover for a ceramic  
semiconductor package comprising:

providing a core comprising iron or iron-nickel  
alloy;

35 applying onto said core a first layer comprising  
nickel, tin, silver, cadmium, indium, lead, copper,  
cobalt, ruthenium, iridium, zinc, and alloys thereof; and



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1           applying a second layer onto said first layer  
comprising palladium, tin, platinum, silver, cadmium,  
indium, cobalt, lead, rhodium, ruthenium, iridium, and  
alloys thereof.

5

22. A method according to claim 21 further  
comprising applying a layer of gold onto said second  
layer.

10

23. A method according to claim 21 wherein said core  
comprises one of Alloy 42, Alloy 45, Alloy 46 and Kovar.

15

24. A method according to claim 21 wherein said  
first layer comprises one from the group consisting of  
electrolytic and electroless nickel and alloys of nickel  
and is applied in a thickness of 100 to 800  $\mu$ in.

20

25. A method according to claim 22 wherein said  
second layer is applied in a thickness of 20 to 60  $\mu$ in.

26. A method according to claim 21 wherein said  
second layer comprises an alloy of palladium and nickel.

25

27. A method according to claim 24 wherein said  
second layer is applied in a thickness of 10 to 100  $\mu$ in.

28. A method according to claim 25 wherein said  
second layer is applied in a thickness of 20 to 60  $\mu$ in.

30

29. A method according to claim 25 wherein said  
second layer comprises an alloy of 80% palladium and 20%  
nickel, by weight.

35

30. A method according to claim 21 wherein said  
second layer comprises at least about 30 wt.% Pd, the  
balance, Ni, Sn or Ag.

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1           31. A method of making a cover for a ceramic semiconductor package comprising:

              providing a core comprising iron or iron-nickel alloy;

5           applying onto said core a first layer comprising nickel or nickel alloy; and

              applying a second layer onto said first layer comprising palladium or palladium alloy.

10           32. A method according to claim 31 further comprising applying a layer of gold onto said second layer.

15           33. A method according to claim 31 wherein said core comprises one of Alloy 42, Alloy 45, Alloy 46 and Kovar.

20           34. A method according to claim 31 wherein said first layer comprises one from the group consisting of electrolytic and electroless nickel and alloys of nickel and is applied in a thickness of 100 to 800  $\mu$ in.

              35. A method according to claim 31 wherein said second layer comprises an alloy of palladium and nickel.

25           36. A method according to claim 31 wherein said second layer is applied in a thickness of 20 to 60  $\mu$ in.

              37. A method according to claim 31 wherein said second layer is applied in a thickness of 10 to 100  $\mu$ in.

30

              38. A method according to claim 31 wherein said second layer is applied in a thickness of 20 to 60  $\mu$ in.

35           39. A method according to claim 31 wherein said second layer comprises an alloy of 80% palladium and 20% nickel, by weight.

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1           40. A soldered, hermetically sealed semiconductor  
package comprising a ceramic enclosure having a  
semiconductor device therein and a cover soldered to the  
ceramic enclosure to hermetically seal said ceramic  
5 enclosure, said cover including a core comprising an iron  
or iron-nickel alloy, a first layer on said substrate  
comprising nickel, tin, silver, cadmium, indium, lead,  
copper, cobalt, ruthenium, iridium, zinc, and alloys  
thereof, a second layer on said first layer comprising  
10 palladium, tin, platinum, silver, cadmium, indium, cobalt,  
lead, rhodium, ruthenium, iridium, and alloys thereof,  
said cover being soldered to said ceramic enclosure with  
a gold-free solder selected from the group consisting of  
solders containing at least one of Pb, Sn, Ab, In, Bi, Pd,  
15 Pt and Sb, and which has a melting point in the range of  
from about 220°C to 300°C.

          41. A package according to claim 40 wherein said  
cover further comprises a coating of gold on said second  
20 layer.

          42. A soldered, hermetically sealed semiconductor  
package according to claim 40 wherein said core comprises  
one of Alloy 42, Alloy 45, Alloy 46 and Kovar.  
25

          43. A soldered, hermetically sealed semiconductor  
package according to claim 40 wherein said first layer  
comprises 100 to 800  $\mu$ in of one from the group consisting  
of electrolytic and electroless nickel and alloys of  
30 nickel.

          44. A soldered, hermetically sealed semiconductor  
package according to claim 40 wherein said first layer is  
400 to 600  $\mu$ in.  
35

          45. A soldered, hermetically sealed semiconductor  
device according to claim 40 wherein said second layer

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1 comprises at least about 30 wt.% Pd, the balance at least  
one from the group consisting of Ni, Ag and Sn.

5 46. A soldered, hermetically sealed semiconductor  
package according to claim 41 wherein said second layer  
comprises 10 to 100  $\mu$ in of one from the group consisting  
of palladium and alloys of palladium.

10 47. A soldered, hermetically sealed semiconductor  
package according to claim 45 wherein said second layer  
comprises an alloy of palladium and nickel.

15 48. A soldered, hermetically sealed semiconductor  
package according to claim 46 wherein said second layer  
comprises an alloy of 80% palladium and 20% nickel, by  
weight.

20 49. A soldered, hermetically sealed semiconductor  
package according to claim 46 wherein said second layer  
comprises 20 to 60  $\mu$ in of an alloy of palladium and  
nickel.

25 50. A soldered, hermetically sealed semiconductor  
package according to claim 41 wherein said solder  
comprises in wt.% about 75% Sn, 20% Ag and 5% Sb.

30 51. A soldered, hermetically sealed semiconductor  
package according to claim 41 wherein said solder  
comprises in wt.% about 84.5% Pb, 5.5% In, 5% Sn, 3% Sb  
and 2% Ag.

35 52. A soldered, hermetically sealed semiconductor  
package according to claim 41 wherein said solder  
comprises about 95 wt.% Pb and about 5 wt.% Pd.

53. A soldered, hermetically sealed semiconductor  
package according to claim 41 wherein said solder

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1 comprises up to about 95% Pb, up to about 5% Pd, up to  
about 5% Ag, up to about 5% Bi, up to about 5% Sb, up to  
5% Au, and up to about 7% of a mixture of Au and Sn having  
up to about 5% Au and up to 2% Sn.

5

54. A soldered, hermetically sealed semiconductor  
package comprising a ceramic enclosure having a  
semiconductor device therein and a cover soldered to the  
ceramic enclosure to hermetically seal said ceramic  
10 enclosure, said cover including a core comprising an iron  
or iron-nickel alloy, a first layer on said substrate  
comprising nickel or nickel alloy, a second layer on said  
first layer comprising palladium or palladium alloy, said  
cover being soldered to said ceramic enclosure with a  
15 gold-free solder selected from the group consisting of  
solders containing at least one of Pb, Sn, Ag, In, Pd, Pt,  
Bi and Sb, and which has a melting point in the range of  
from about 220°C to 300°C.

20

55. A package according to claim 54 wherein said  
cover further comprises a coating of gold on said second  
layer.

25

56. A soldered, hermetically sealed semiconductor  
package according to claim 54 wherein said core comprises  
one of Alloy 42, Alloy 45, Alloy 46 or Kovar.

30

57. A soldered, hermetically sealed semiconductor  
package according to claim 54 wherein said first layer  
comprises 100 to 800  $\mu$ in of one from the group consisting  
of electrolytic and electroless nickel and alloys of  
nickel.

35

58. A soldered, hermetically sealed semiconductor  
package according to claim 56 wherein said first layer is  
400 to 600  $\mu$ in.

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1           59. A soldered, hermetically sealed semiconductor  
package according to claim 54 wherein said second layer  
comprises at least about 30 wt.% Pd, the balance at least  
one of Ni, Ag and Sn.

5

60. A soldered, hermetically sealed semiconductor  
package according to claim 54 wherein said second layer  
comprises 10 to 100  $\mu$ in of one from the group consisting  
of palladium and alloys of palladium.

10

61. A soldered, hermetically sealed semiconductor  
package according to claim 58 wherein said second layer  
comprises an alloy of palladium and nickel.

15

62. A soldered, hermetically sealed semiconductor  
package according to claim 60 wherein said second layer  
comprises an alloy of 80% palladium and 20% nickel, by  
weight.

20

63. A soldered, hermetically sealed semiconductor  
package according to claim 60 wherein said second layer  
comprises 20 to 60  $\mu$ in of an alloy of palladium and  
nickel.

25

64. A soldered, hermetically sealed semiconductor  
package according to claim 54 wherein said solder  
comprises in wt.% about 75% Sn, 20% Ag and 5% Sb.

30

65. A soldered, hermetically sealed semiconductor  
package according to claim 54 wherein said solder  
comprises in wt.% about 84.5% Pb, 5.5% In, 5% Sn, 3% Sb  
and 2% Ag.

35

66. A soldered, hermetically sealed semiconductor  
package according to claim 54 wherein said solder  
comprises in wt.% about 95% Pb and about 5% Pd.

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1           67. A sealing cover consisting essentially of an  
iron and nickel alloy core, a 400  $\mu$ in thick first layer of  
material from the group consisting of nickel, tin, silver,  
cadmium, indium, lead, copper, cobalt, ruthenium, iridium,  
5       zinc, and alloys thereof, a 20-60  $\mu$ in second layer of a  
material from the group consisting of palladium, tin,  
platinum, silver, cadmium, indium, cobalt, lead, rhodium,  
ruthenium, iridium, and alloys thereof and a layer of 0 to  
15  $\mu$ in of gold on the second layer.

10

68. A sealing cover consisting essentially of an  
iron and nickel alloy core, a 400  $\mu$ in thick first layer of  
material from the group consisting of nickel and nickel  
alloys, a 20-60  $\mu$ in second layer of a material from the  
15       group consisting of palladium and palladium-nickel alloys  
and a layer of 0 to 15  $\mu$ in of gold on the second layer.

69. A method of making a sealing cover comprising  
providing a core of an alloy of iron and nickel, applying  
20       a first layer to the core comprising nickel or nickel  
alloy of 100 to 800  $\mu$ in thickness and applying a second  
layer onto the first layer of palladium or palladium-  
nickel alloy of 10 to 100  $\mu$ in thickness.

25           70. A method according to claim 68 further  
comprising applying a layer of gold of 0 to 15  $\mu$ in  
thickness onto the second layer.

71. A method according to claim 68 wherein said  
30       first layer is applied as a layer of 400 to 600  $\mu$ in  
thickness.

72. A method according to claim 68 wherein said  
second layer is applied as a layer of 20 to 60  $\mu$ in  
35       thickness.

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1           73. A method according to claim 68 wherein said  
first layer is electrolytic nickel.

5           74. A method according to claim 68 wherein said  
second layer is applied as a layer of at least 30%  
palladium, the balance nickel.

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## AMENDED CLAIMS

[received by the International Bureau on 6 September 1994 (06.09.94);  
original claim 3 amended;  
other claims unchanged (1 page)]

1

1. A solderable metallic cover for hermetically sealing a package containing a semiconductor device comprising a core of iron or iron-nickel alloy, a first layer on said core comprising nickel, tin, silver, cadmium, indium, lead, copper, cobalt, ruthenium, iridium, zinc, and alloys thereof, and a second layer on said first layer comprising palladium, tin, platinum, silver, cadmium, indium, cobalt, lead, rhodium, ruthenium, iridium, and alloys thereof, and a layer of gold on said second layer of a thickness of 0 to 50  $\mu\text{in}$ .

15

2. A solderable metallic cover for hermetically sealing a package containing a semiconductor device comprising a core of iron or iron-nickel alloy, a first layer on said core comprising nickel or nickel alloy, and a second layer on said first layer comprising palladium or palladium alloy and a layer of gold on said second layer of a thickness of 0 to 50  $\mu\text{in}$ .

20

25

3. A cover according to claim 2 wherein said core comprises one of Alloy 42, Alloy 45, Alloy 46 or Kovar.

30

4. A cover according to claim 2 wherein said first layer comprises one from the group consisting of electrolytic and electroless nickel and alloys of nickel of a thickness of 100 to 800  $\mu\text{in}$ .

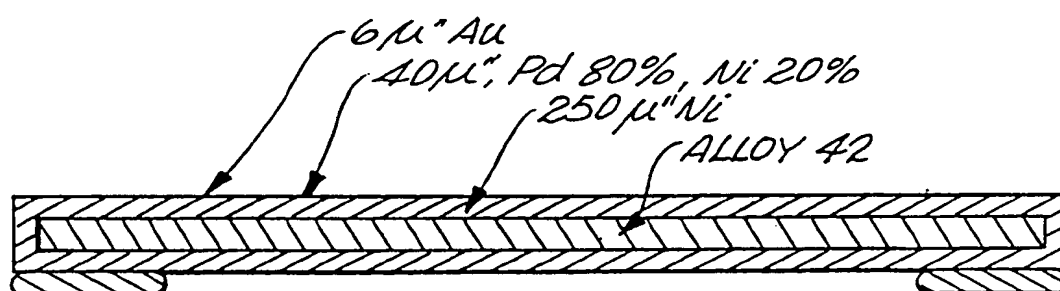
35

5. A cover according to claim 4 wherein said first layer is 400 to 600  $\mu\text{in}$ .

6. A cover according to claim 2 wherein said second layer comprises at least about .30 wt.% palladium, the balance nickel, silver or tin.

*Fig. 2*

EXAMPLE OF NEW LID



## INTERNATIONAL SEARCH REPORT

International application No.,  
PCT/US94/03788

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H01L 23/02, 21/465; H05K 5/06; H01S 4/00

US CL :Please See Extra Sheet.

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 174/52.2, 52.3, 52.4; 257/678, 699,704; 437/225, 245, 246; 29/592.1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

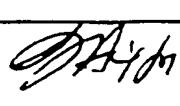

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A, 5,045,639 (Liu et al.) 03 September 1991, Fig. 2	1
Y	US,A,4,842,961 (Basile et al.) 27 JUNE 1989, claims 1-15	1-74
Y	US,A,4,737,418 (Slattery) 12 APRIL 1988, Figs. 4-6	1-74
Y	US,A,4,666,796 (Levine) 19 MAY 1987, entire document	1-74
Y	US,A,4,835,067 (Levine) 30 MAY 1989, entire document	1-74
Y	US,A,4,640,438 Trevison et al.) 03 FEBRUARY 1987, Figs. 1-2	1-74

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier document published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 22 JUNE 1994	Date of mailing of the international search report 07 JUL 1994
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer  BOT LEDYNH Telephone No. (703) 308-0225 

Form PCT/ISA/210 (second sheet)(July 1992)\*

# INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US94/03788

## C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,A,4,640,436 (Miyoshi et al.) 03 FEBRUARY 1987, Figs. 1-3	1-74
Y	US,A,4,601,958 (Levine) 22 JULY 1986, entire document	1-74
Y	US,A,4,331,253 (Gordon et al.) 25 MAY 1982, col. 3, lines 1-49	1-74
Y	US,A,4,331,258 (Geschwind) 25 MAY 1982, entire document	1-74
Y	US,A,4,141,029 (DROMSKY) 20 february 1979, Fig. 3	1-74

Form PCT/ISA/210 (continuation of second sheet)(July 1992)\*

# INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US94/03788

## A. CLASSIFICATION OF SUBJECT MATTER: US CL :

174/52.2, 52.3, 52.4; 257/678, 699,704; 437/225, 245, 246; 29/592.1

*Fig. 2* EXAMPLE OF NEW LID

